TRUNCATION SCHEMES FOR
RECURSIVE MULTIPLIERS

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Outline

• Motivation & Objectives
• Recursive Digital Multipliers
• Existing Truncation Methods
• Proposed Truncation Schemes for Recursive Multipliers
• Simulation Results
• Conclusions
Motivation

• Constant word size is required throughout arithmetic operations, i.e. DSP applications

• Rounding circuitry can be complex

• Various truncations schemes have been presented for multipliers
  • Significant reduction in complexities

• Most existing schemes target array and tree multipliers

• The inherent structure of the digital recursive multiplier is very suitable for truncation
Objectives

• Error Analysis:
  • Eliminating a portion of the digital recursive multiplier
  • Proposed truncation schemes

• Gate Complexity Analysis
Recursive Digital Multipliers

- Recursive, or “divide and conquer” multiplication was proposed by Karatsuba and Ofman in 1962

- The Karatsuba-Ofman Algorithm (KOA) multiplies two long integers by executing multiplications and additions on their divided parts

- Fundamental principles of KOA is utilized in the recursive algorithm [Danysh and Swartzlander]
Recursive Digital Multipliers

• Mathematically, the recursive algorithm is established around the fact that any $2n \times 2n$ bit multiplication can be carried out through four $n \times n$ bit sub-multiplications

• Considering two unsigned $2n$-bit operands:

  \[
  \text{Multiplicand: } A = A_H \times 2^n + A_L \\
  \text{Multiplier: } X = X_H \times 2^n + X_L \\
  \text{Product: } Y = A \cdot X = (A_H \times 2^n + A_L) \cdot (X_H \times 2^n + X_L) \\
  \hspace{1cm} = A_H X_H \times 2^{2n} + (A_L X_H + A_H X_L) \times 2^n + A_L X_L
  \]
Recursive Digital Multipliers

- Block diagram representation for multiplication with a single level of recursion
- $Y$ is the fixed-width rounded product of $2n$ bits
Recursive Digital Multipliers

- Of the 4 sub-multiples, the one contributing the least to the final product is $A_L \times X_L$
- Truncation schemes to be presented will target this particular component
Existing Truncation Methods

- Truncation schemes generally involve not generating the complete partial product matrix in a multiplication, and then applying a scheme to compensate for the error.

- Correction schemes:
  - Constant Correction [Y. C. Lim]
  - Variable Correction [E. J. King and E. E. Swartzlander, Jr.]
Existing Truncation Methods

• Constant Correction
  • A constant is added to the remaining columns of the partial products matrix based on average value of the bits which are not formed and expected value of rounding error

• Variable Correction
  • Correction value is data dependent:
    - If all elements are zeros in the most significant column not formed, there is no correction
    - If all elements are ones, then a maximum correction value is used

• Variable correction results in a lower variance in error
• Constant correction is efficiently implemented with tree multipliers and variable correction with array multipliers
Proposed Truncation Schemes for Digital Recursive Multipliers

- Three truncation schemes targeting recursive multipliers involving data-dependent correction terms are proposed.

- Original recursive multiplier can be represented in this way:

\[
\begin{array}{c}
2n \\
A_H \times X_L \\
A_H \times X_H \\
A_L \times X_L \\
A_L \times X_H \\
\end{array}
\]

- The component \(A_L X_L\) will be truncated.
Proposal #1 Truncation Scheme

- $A_H X_L$ or $A_L X_H$ is simply used to replace the truncated term $A_L X_L$:

  \[
  \begin{align*}
  &\underbrace{A_H \times X_L}^{2n} \\
  &\underbrace{A_H \times X_H} \quad \underbrace{A_H X_L} \\
  &\underbrace{A_L \times X_H}
  \end{align*}
  \]

- This correction term is generated at no extra cost
Proposal #2 Truncation Scheme

• The average of the two blocks $A_H X_L$ and $A_L X_H$ replaces $A_L X_L$:

$$\frac{A_H X_L + A_L X_H}{2}$$

• High correlation between the truncated term and the replacement term
Proposal #3 Truncation Scheme

- Partial product bit \( a_{n-1}x_{n-1} \) (MSB generated in \( A_LX_L \)) is added at the least significant bit position of block \( A_HX_H \):

\[
\begin{align*}
A_L &= a_{n-1}a_{n-2}...a_2a_1a_0 \\
X_L &= x_{n-1}x_{n-2}...x_2x_1x_0
\end{align*}
\]

- A 1-bit correction term is generated with little extra cost
- Simplifies the partial products accumulation step
Simulation Results

- **Error Statistics**: Comparison with existing truncation techniques (6-bit recursive multiplier)

<table>
<thead>
<tr>
<th>Multiplier Type</th>
<th>Mean Error</th>
<th>Max. Positive Error</th>
<th>Max. Negative Error</th>
<th>Variance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Truncation</td>
<td>-0.469</td>
<td>0.000</td>
<td>-0.984</td>
<td>0.086</td>
</tr>
<tr>
<td>True Rounding</td>
<td>0.000</td>
<td>0.500</td>
<td>-0.500</td>
<td>0.083</td>
</tr>
<tr>
<td>Constant Correction 1</td>
<td>0.4</td>
<td>1</td>
<td>-4</td>
<td>0.2</td>
</tr>
<tr>
<td>Constant Correction 2</td>
<td>-0.06</td>
<td>3</td>
<td>-2</td>
<td>0.2</td>
</tr>
<tr>
<td>Variable Correction</td>
<td>0.06</td>
<td>1.4</td>
<td>-0.9</td>
<td>0.1</td>
</tr>
<tr>
<td>Removal of $A_LX_L$</td>
<td>-0.191</td>
<td>0.500</td>
<td>-1.266</td>
<td>0.128</td>
</tr>
<tr>
<td>Proposal #1</td>
<td>-0.000</td>
<td>1.141</td>
<td>-1.156</td>
<td>0.128</td>
</tr>
<tr>
<td>Proposal #2</td>
<td>0.037</td>
<td>0.875</td>
<td>-0.906</td>
<td>0.109</td>
</tr>
<tr>
<td>Proposal #3</td>
<td>0.059</td>
<td>1.250</td>
<td>-0.828</td>
<td>0.173</td>
</tr>
</tbody>
</table>

Table 1. Error Statistics ($2n = 6$)
**Simulation Results**

- **Complexity Comparison**: Savings in number of gates
- It is assumed that base multiplier for the recursive structure is array multiplier
- Estimate one full adder as 12 gates, one half adder as 4 gates

<table>
<thead>
<tr>
<th>(2n)</th>
<th>Original</th>
<th>Proposal #1</th>
<th>Proposal #2</th>
<th>Proposal #3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>No. of Gates</td>
<td>No. of Gates</td>
<td>% Savings</td>
<td>No. of Gates</td>
</tr>
<tr>
<td>8</td>
<td>812</td>
<td>712</td>
<td>12</td>
<td>852</td>
</tr>
<tr>
<td>16</td>
<td>3196</td>
<td>2600</td>
<td>19</td>
<td>2884</td>
</tr>
<tr>
<td>32</td>
<td>12956</td>
<td>10120</td>
<td>22</td>
<td>10692</td>
</tr>
<tr>
<td>64</td>
<td>52444</td>
<td>40136</td>
<td>24</td>
<td>41284</td>
</tr>
</tbody>
</table>

Table 2. Complexity Comparison
Simulation Results

- All three proposed schemes show that they have comparatively low errors.

- In terms of complexity, hardware savings are close to 25% when $n$ is large.

- However, gate number is not always a good metric for overall performance.

- For example, Proposal #2 (averaging of two components) involves an addition of 2 more rows to the partial product matrix, increasing the time required for partial products reduction step.

- Further hardware reduction is expected if these correction schemes are applied to multi-level recursive multipliers.
Multi-level Recursive Multiplier

- Maximum complexity savings after truncation of least significant sub-multiple:

<table>
<thead>
<tr>
<th>Levels of Recursion</th>
<th>Projected Maximum Complexity Savings (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>25.0</td>
</tr>
<tr>
<td>2</td>
<td>37.5</td>
</tr>
<tr>
<td>3</td>
<td>43.8</td>
</tr>
</tbody>
</table>
Conclusions

• Three reduced-hardware truncation schemes have been proposed, targeting the very regular composition of recursive multipliers

• Examination of hardware overhead and truncation error trade-off allows for the proper selection of a scheme

• These are the initial results of an on-going investigation on reduced-hardware truncations schemes with error correction schemes
Thank you for your attention!