Algebraic Integer Encoding and Applications in Discrete Cosine Transform

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Feb. 3rd, 2004

OUTLINE

- Algebraic Integer DCT Encoding
- DCT IP Core Design and Fabrication
- Simulation Results and Chip Testing
- Conclusion

DCT

DCT:

1-D DCT:

$$F(k)=\sum_{n=0}^{N-1}x(n)\cdot\cos\left(\frac{(2n+1)k}{2N}\pi\right) \quad 1\le k\le N-1;$$

2-D DCT:

$$F(k,l)=\sum_{m=0}^{N-1}\sum_{n=0}^{N-1}x(m,n)\cdot\cos\left(\frac{(2n+1)k}{2N}\pi\right)\cos\left(\frac{(2m+1)l}{2N}\pi\right);$$

$$1\le k\le N-1 \quad 1\le l\le N-1$$

Properties and Applications:

- DCT has energy packing capabilities and also approaches the statistically optimal transform in de-correlating a signal governed by Markov Process.
- DCT is orthogonal and separable, it leads to the reduction of spatial redundancy for the input signal and has found wide applications in speech and image processing.
- The 2-Dimensional DCT, over a small block of pixels, has been widely used as a frequency analysis and compression algorithm in image processing standard like MPEG-2.

Algebraic Integer DCT Encoding

$$Z_1 = 2\cos(1\cdot\pi/16)$$

$$f(Z_1) = \sum_{i=0}^{7} a_i Z_1^{\,i}$$

	a_0	a_1	a_2	a_3	a_4	a_5	a_6	a_7	Error
$2\cos(0\cdot\pi/16)$	2	0	0	0	0	0	0	0	0
$2\cos(1\cdot\pi/16)$	0	1	0	0	0	0	0	0	0
$2\cos(2\cdot\pi/16)$	-2	0	1	0	0	0	0	0	0
$2\cos(3\cdot\pi/16)$	0	-3	0	1	0	0	0	0	0
$2\cos(4\cdot\pi/16)$	2	0	-4	0	1	0	0	0	0
$2\cos(5\cdot\pi/16)$	0	5	0	-5	0	1	0	0	0
$2\cos(6\cdot\pi/16)$	-2	0	9	0	-6	0	1	0	0
$2\cos(7\cdot\pi/16)$	0	-7	0	14	0	-7	0	1	0

Table I: 1D Algebraic Integer Encoding for 8 Point DCT

$$z_1 = 2\cos(\pi/16) \quad z_2 = 2\cos(4\pi/16)$$

$$f(z_1, z_2) = \sum_{i=0}^{3}\sum_{j=0}^{1} a_{ij} z_1^{\,i} z_2^{\,j}$$

$2\cos(0\cdot\pi/16)$	$\begin{bmatrix} 2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	$2\cos(1\cdot\pi/16)$	$\begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$
$2\cos(2\cdot\pi/16)$	$\begin{bmatrix} -2 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	$2\cos(3\cdot\pi/16)$	$\begin{bmatrix} 0 & -3 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}$
$2\cos(4\cdot\pi/16)$	$\begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}$	$2\cos(5\cdot\pi/16)$	$\begin{bmatrix} 0 & 3 & 0 & -1 \\ 0 & 1 & 0 & 0 \end{bmatrix}$
$2\cos(6\cdot\pi/16)$	$\begin{bmatrix} 2 & 0 & -1 & 0 \\ -2 & 0 & 1 & 0 \end{bmatrix}$	$2\cos(7\cdot\pi/16)$	$\begin{bmatrix} 0 & -1 & 0 & 0 \\ 0 & -3 & 0 & 1 \end{bmatrix}$

Table II: 2D Algebraic Integer Encoding for 8 Point DCT

Exploiting Redundancy – Zero Pattern

$$F(k)=\sum_{n=0}^{N-1}x(n)\cdot\cos\left(\frac{(2n+1)k}{2N}\pi\right);$$

$$F(2k')=\sum_{n=0}^{N-1}x(n)\cdot\cos\left(\frac{(2n+1)2k'}{2N}\pi\right);$$

$$F(2k'+1)=\sum_{n=0}^{N-1}x(n)\cdot\cos\left(\frac{(2n+1)(2k'+1)}{2N}\pi\right);$$

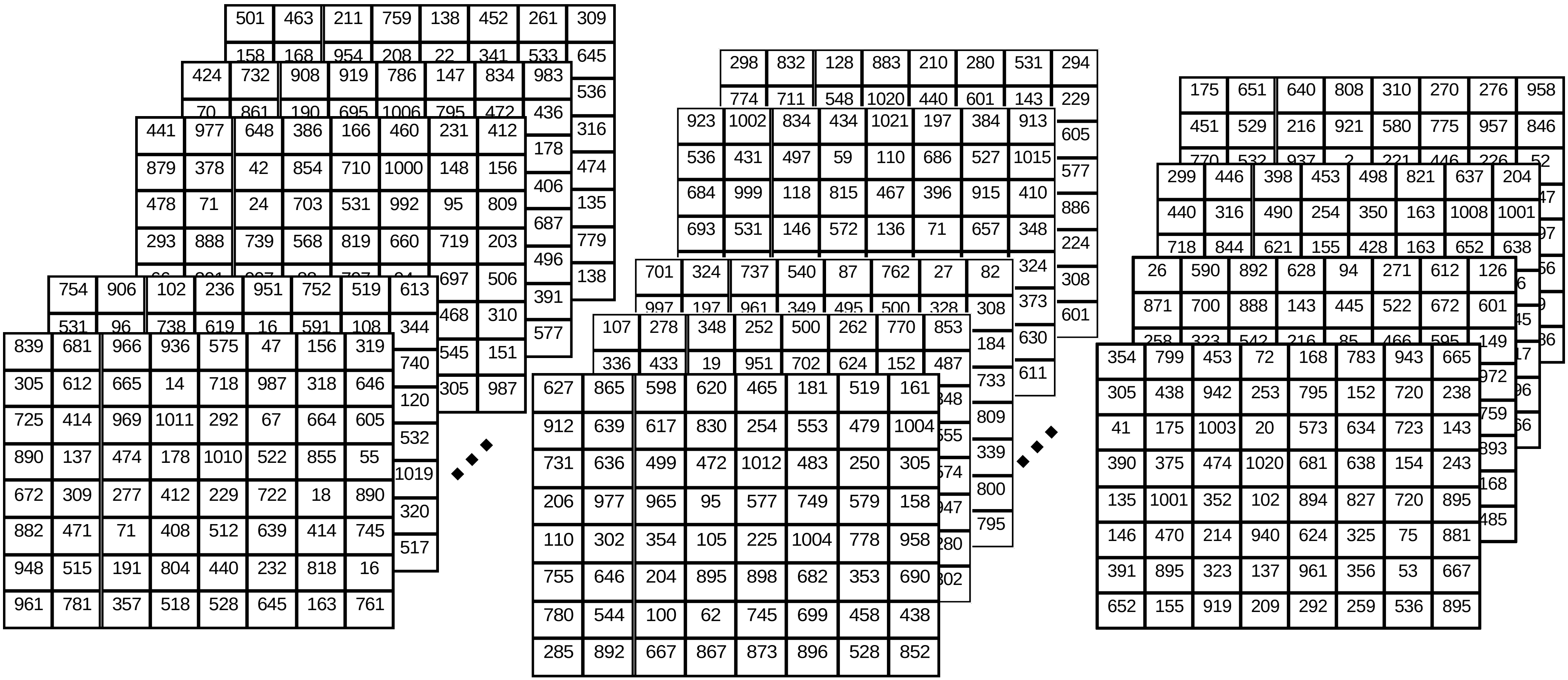
$$F(0,2,4,6)$$

$$F(1,3,5,7)$$

$$\left\{\cos\left(\frac{0\pi}{16}\right),\cos\left(\frac{2\pi}{16}\right),\cos\left(\frac{4\pi}{16}\right),\cos\left(\frac{6\pi}{16}\right)\right\}$$

$$\left\{\cos\left(\frac{1\pi}{16}\right),\cos\left(\frac{3\pi}{16}\right),\cos\left(\frac{5\pi}{16}\right),\cos\left(\frac{7\pi}{16}\right)\right\}$$

Exploiting Redundancy – Zero Pattern



2D implementation:

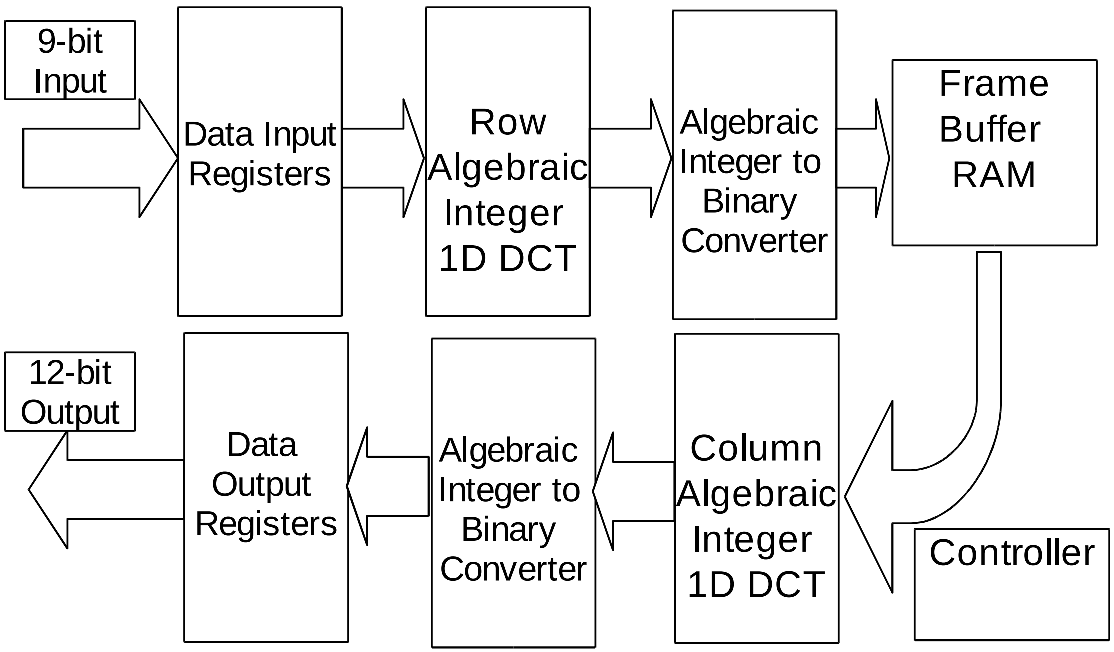
15 layers of algebraic integer representation

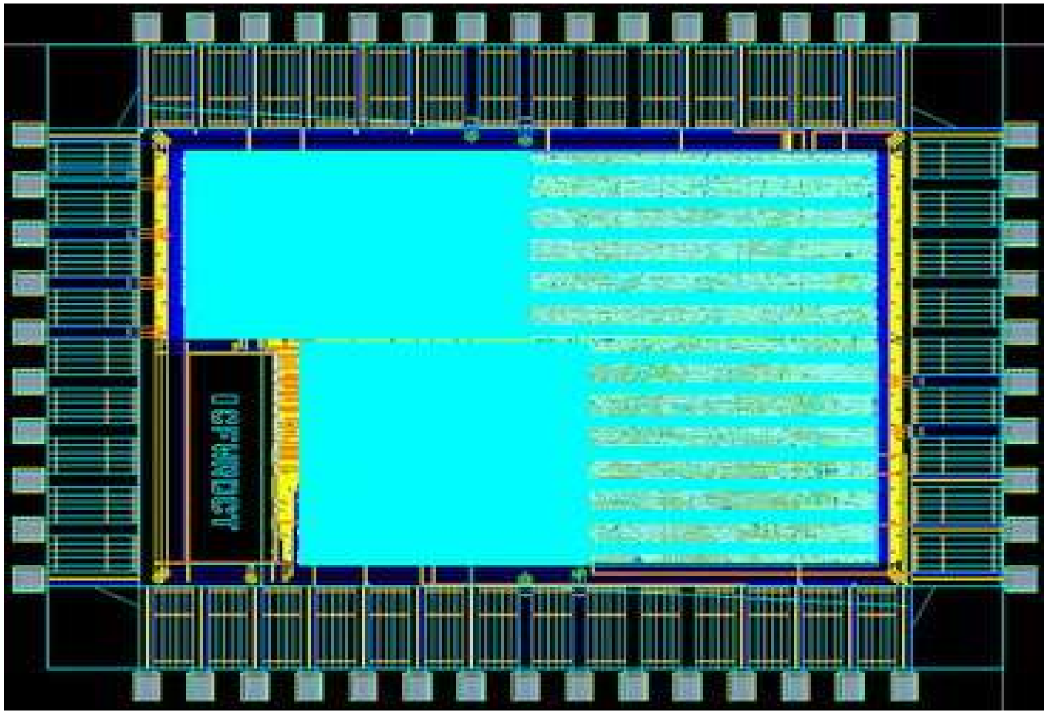
1D implementation:

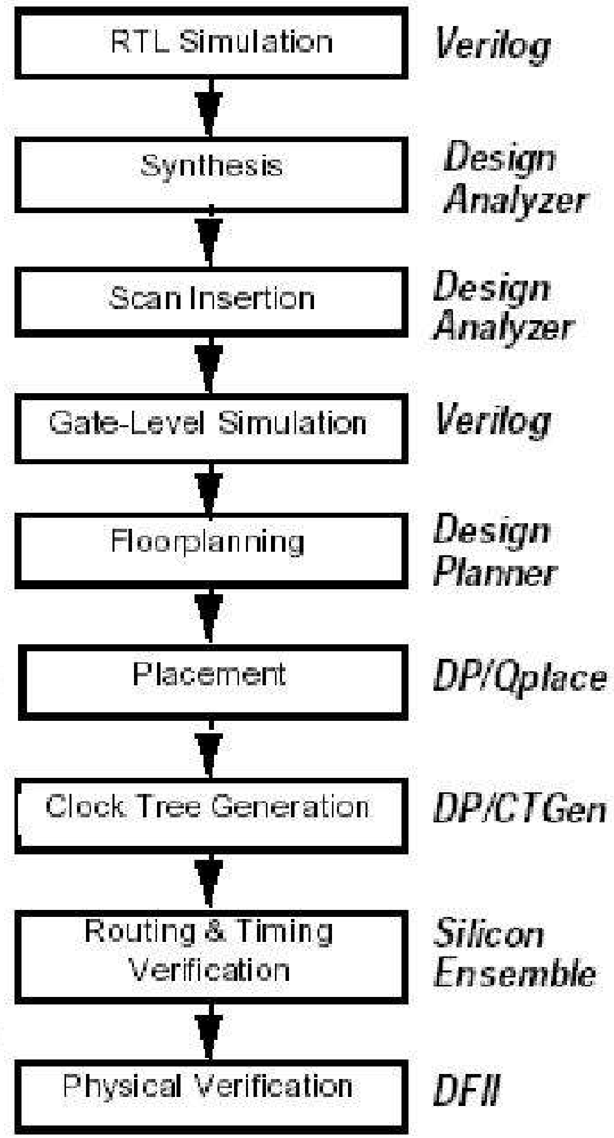
8 layers of algebraic integer representation

Zero Pattern:

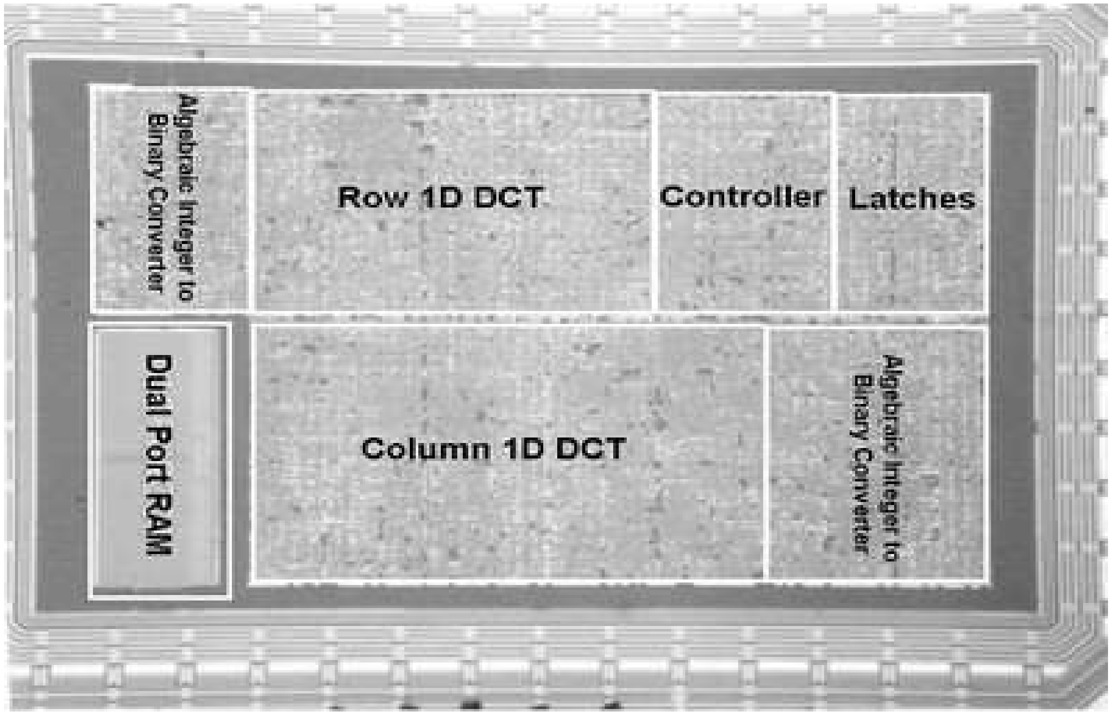
4 layers of algebraic integer representation







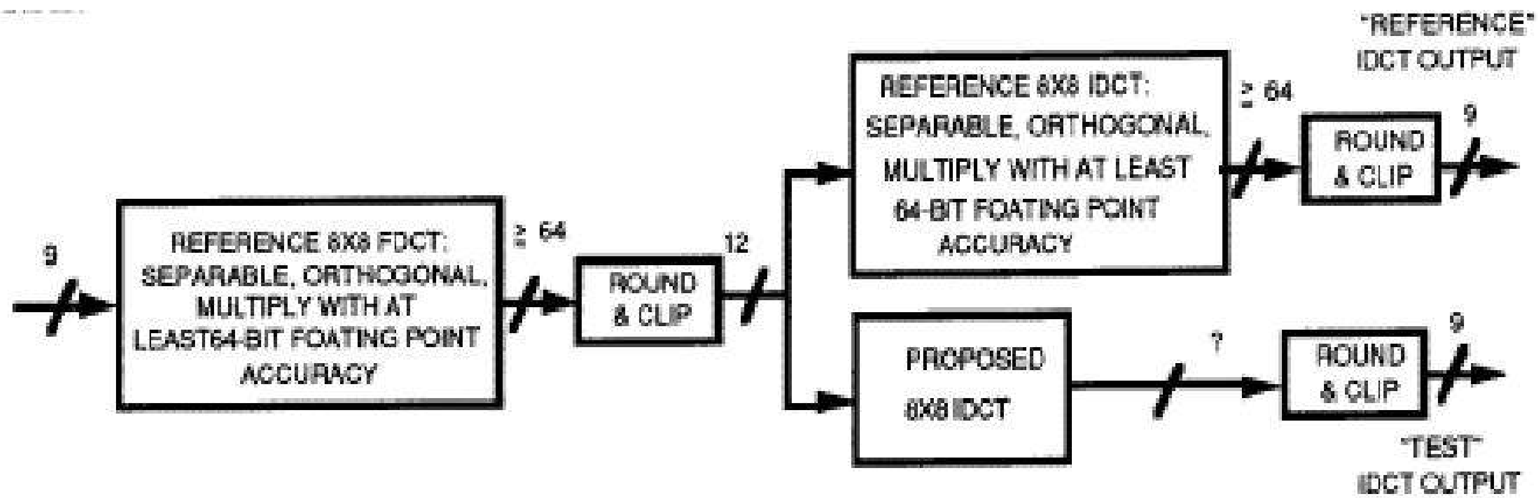
Design Architecture, Flow, Tools and Chip Layout



• Function	two-dimensional 8x8 DCT
• Inputs / Outputs	9 bit signed(pixel)/12 bit signed (DCT)
• Internal Word-length	10-13 (algebraic integer), 16 (binary)
• Accuracy	IEEE Standard 1180-1990
• Technology	TSMC CMOS 0.18μm
• Core Size	1.8$mm \times$ 1.2mm
• Power Dissipation	7.5mW @ 75MHz/1.2V
• Throughput	75M *pixel/second*
• Latency	80 clock cycles

Algebraic Integer 8x8 DCT Chip Micrograph and Highlights

Simulation Results - numerical characteristics



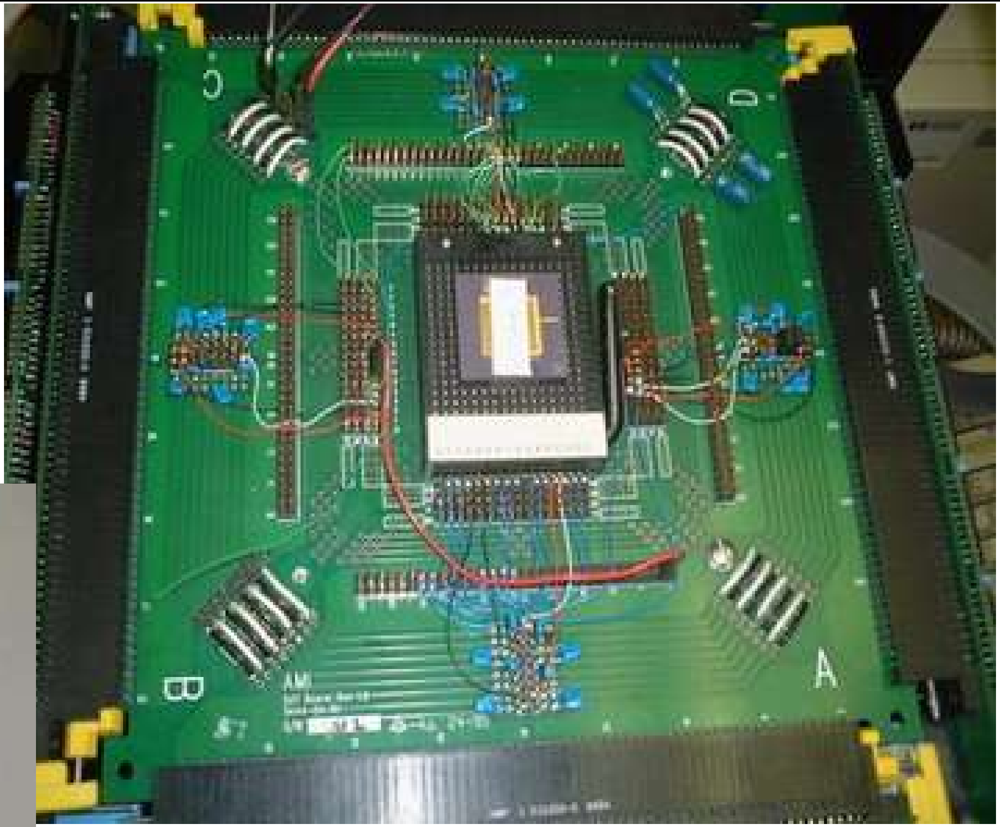
input range	[-256 255]	[-300 300]	[-5 5]	IEEE std.
mppe	<=1	<=1	<=1	<=1
mpmse/mpme	0.055	0.056	0	<=0.06
ome/omse	0.00072	0.00084	0	<=0.0015
zero_test	0	0	0	0

Simulation Results According to IEEE Standard 1180-1990
Using Algebraic Integer Representations

Simulation Results – Power Estimation

Power Consumption for Processing Input Image Blocks of 128x128				
Global Operating Voltage = 1.6/1.2 V				
Operating Speed: 75 MHz Power Unit: mW				
Image \ Design	ICFWRDCT	DCT_Inc_Compile	clock_gating1	clock_gating2
Gauss-random	24.346/13.695	16.766/9.431	17.015/9.571	12.135/6.826
Peppers	8.591/4.832	6.186/3.493	5.099/2.868	4.635/2.607
Lena	8.536/4.802	6.139/3.453	5.034/2.832	4.584/2.579
Bridge	8.500/4.781	6.132/3.449	5.025/2.827	4.577/2.575
Goldh	8.437/4.746	6.081/3.421	4.970/2.796	4.533/2.550
Camera	7.914/4.452	5.707/3.210	4.632/2.606	4.249/2.390
Bird	7.570/4.258	5.442/3.061	4.377/2.462	4.084/2.297

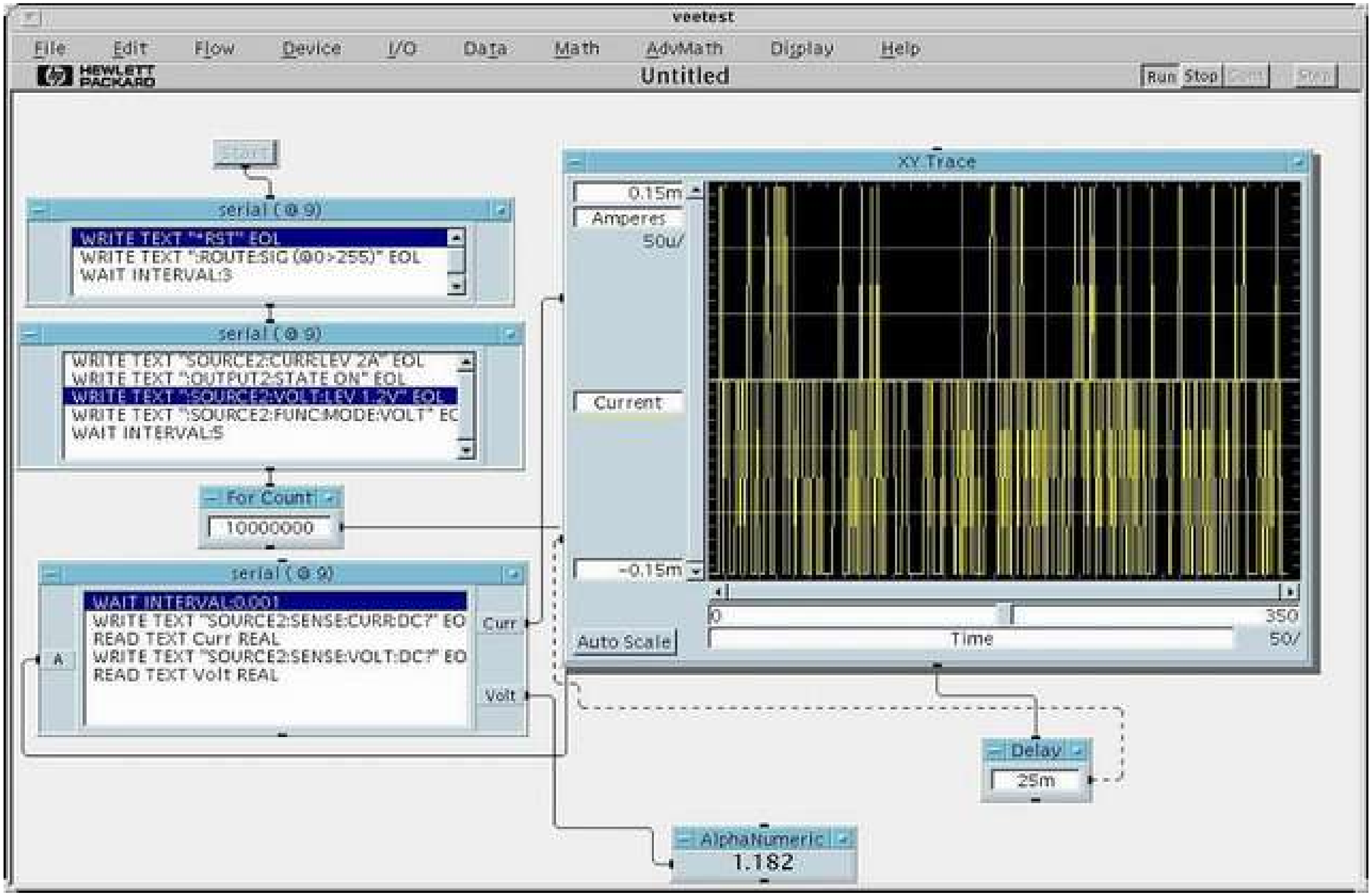
CMC DUT Testing Board on the CMC TH1000 Test Head



Testing Environment

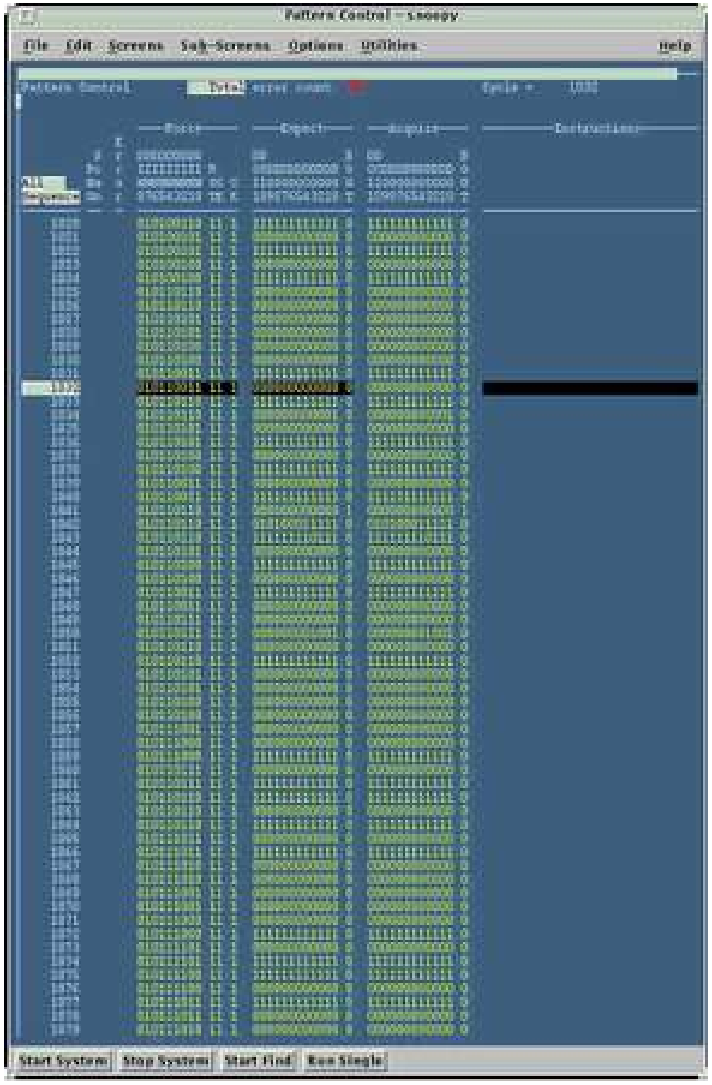
- CMC TH1000 Test Head
- HP 9000/745i workstation with HP-UX A09.01 Operating System
- HP 75000D20, VXI Digital Test System
- HP 6621A DC Power Supplies
- Tektronix 11402 Digital Oscilloscope

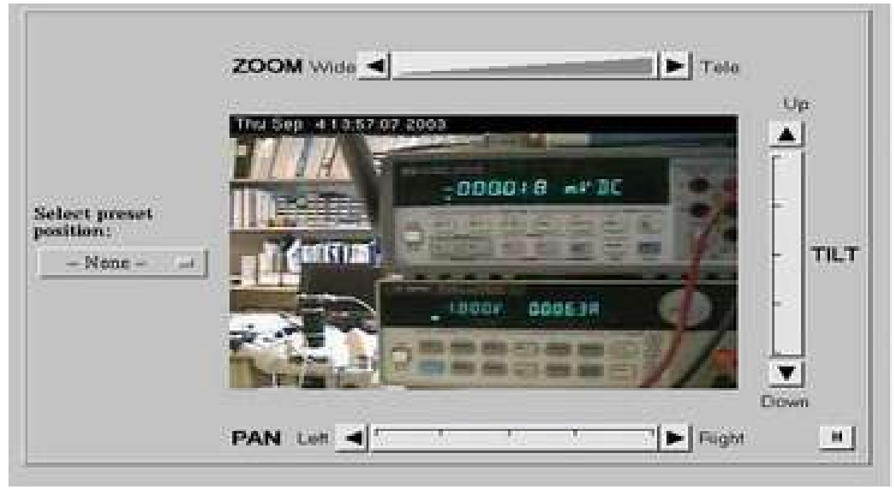
Simulation Results and Chip Testing

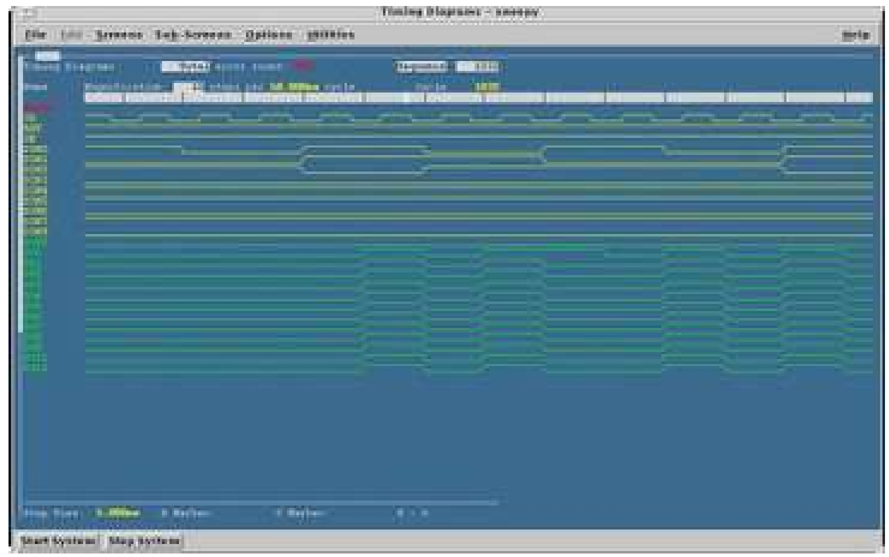


HP Veetest Digital Testing Software Environment

Simulation Results and Chip Testing







IMS Digital Testing System Environment

Simulation Results and Chip Testing

- Functional : Works.
- Test Frequency : 50MHz.
- Power Consumption: 1.8V*0.0063mA = 11.34mW @ 50MHz

  scaling: 1.2V*0.0042mA = 5.04mW @ 50MHz

  7.56mW @ 75MHz

Design	Core Size / Technology	Scaled Power Consumption (mJ/Mpixels)
Xanthopoulos [5]	14.5 mm^2 / 0.6 μm CMOS	0.313
Chang et al. [6]	7.85 $\times$ 6.45 mm^2 / 0.6 μm CMOS	1.38
August et al. [7]	0.35 μm CMOS	0.156
Masera et al. [8]	Xilinx XCV100E	0.527
Proposed Alg_int DCT	1.8 mm $\times$ 1.2 mm / 0.18 μm CMOS	0.1

Testing Results and Power Consumption Comparisons

Conclusion

- The error-free 2D algebraic integer encoding scheme for DCT basis function provide an alternative for DCT computing

- The multiplier-less high-precision feature of the algebraic integer encoding combined with selected suitable DCT algorithm enable an efficient implementation of the 8 x 8 DCT IP core

Publications

[1] Minyi Fu, V.S. Dimitrov and G.A. Jullien, "An Efficient Technique for Error-free Algebraic-integer Encoding for High Performance Implementation of the DCT and IDCT", in Proc. IEEE International Symposium on Circuits and Systems, Sydney Australia, May 2001, pp. 906-909.

[2] M. Fu, M. Ahmadi and W.C.Miller, V.Dimitrov, G.A.Jullien, "Implementation of an Error-free DCT Using Algebraic Integers", Micronet Annual Workshop, Hull Quebec Canada. April, 2002.

[3] Minyi Fu, G.A.Jullien, V.S.Dimitrov, M.Ahmadi, W.C.Miller, "The Application of 2D Algebraic Integer Encoding to a DCT IP Core", The 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications, Calgary, AB Canada, June 30 - July 2, 2003, pp. 66-69.

[4] Minyi Fu, G. A. Jullien, V. S. Dimitrov, M. Ahmadi, “A Low-Power DCT IP Core Based on 2D Algebraic Integer Encoding”, Sumbitted to ISCAS2004.