A Built-in Self-Test for System-on-Chip

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Objective : Design an intellectual property (IP) core which enables low speed Automatic Test Equipment (ATE) to perform test for a System-on- Chip (SoC)

Motive :

Fast SoC market growing

Today SoC accounts for about 20%

Predictions : It will grow to 60% within the next four years.

Cost of testing – ATE:

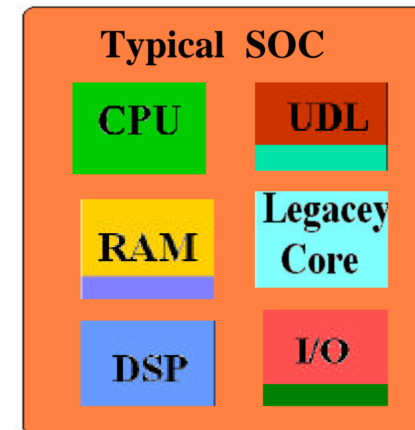
0.5-1.0GHz,1,024 digital pins ATE :

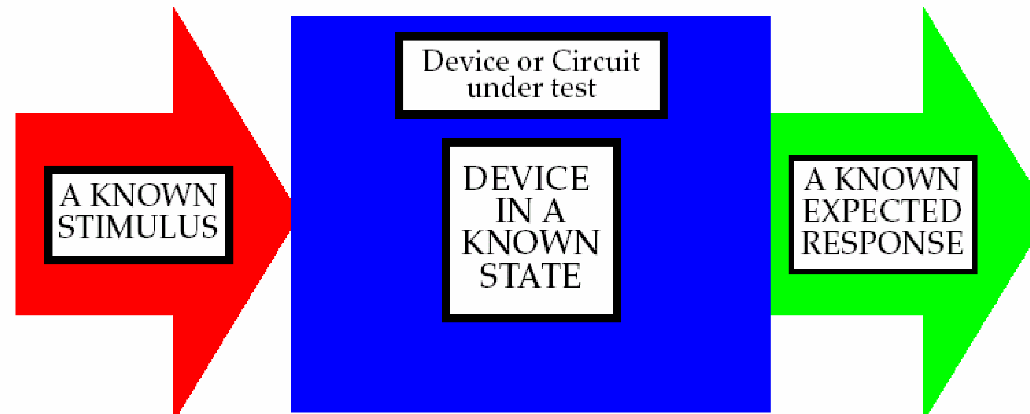
price =$1.2M +1,024 x $3,000 =$4.272M

What is a SoC?

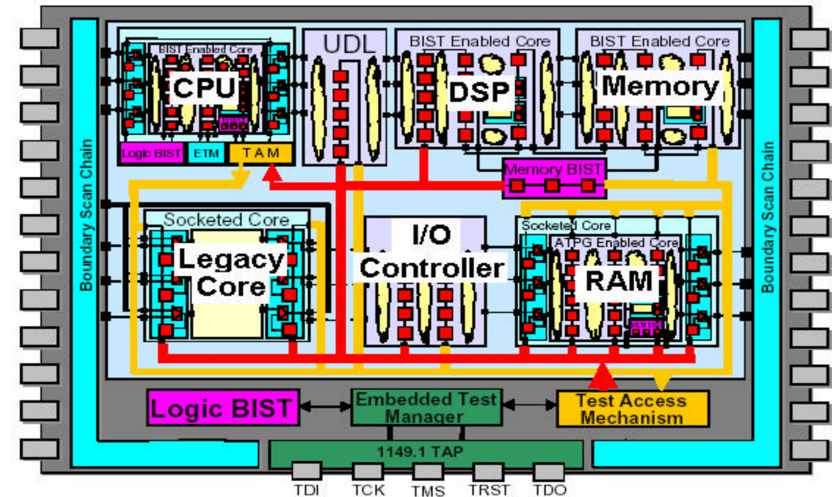
SOC is a complex integrated circuit (IC) that integrates the major functional elements of a complete end-product into a single chip using IP blocks:

* Programmable processor
* Controllers
* Signal processors
* On-chip memory





Design For Test Methodologies

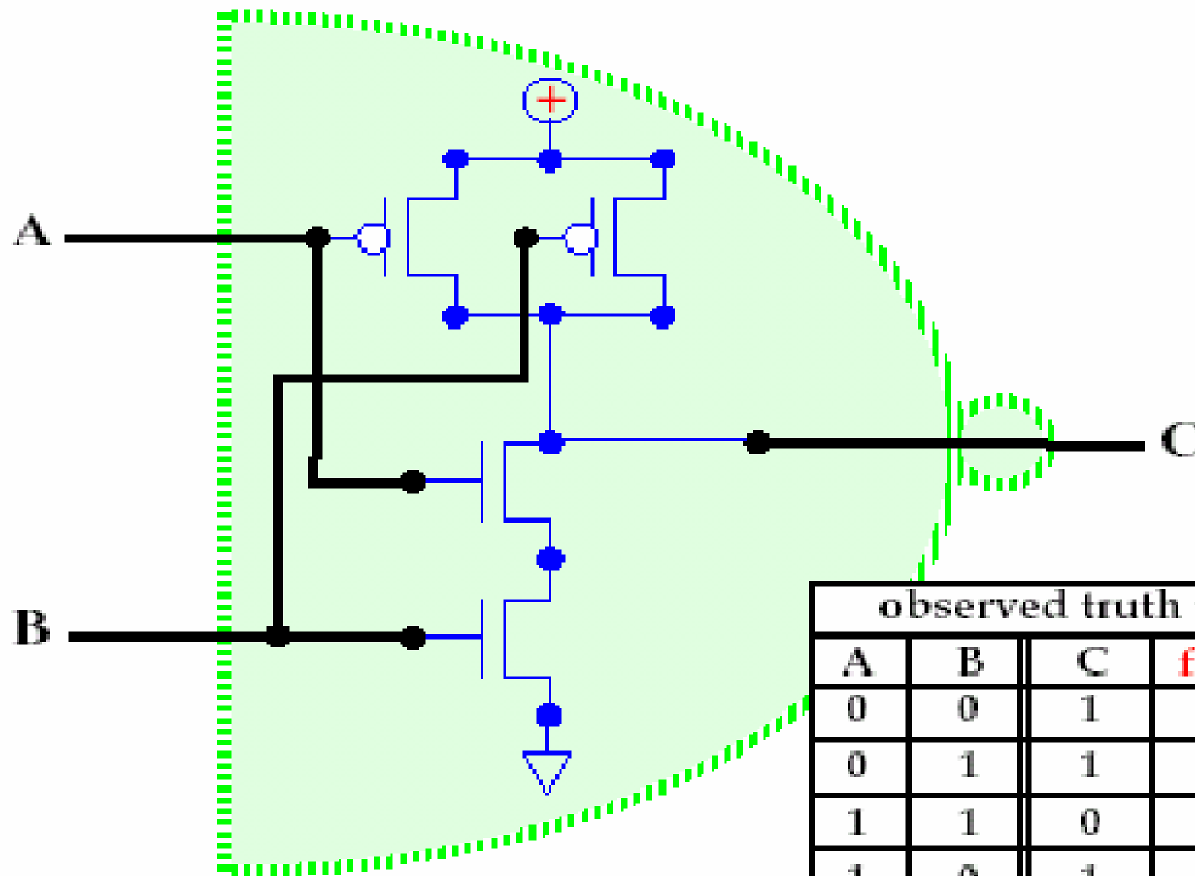


1- Scan Technique
- Partial scan
- Full scan
- Boundary scan
- Scan chain

2- IEEE 1500 Standard for Embedded Core Test
- Test Wrapper

3- Build In Self Test (BIST)

Gate level stuck at faults



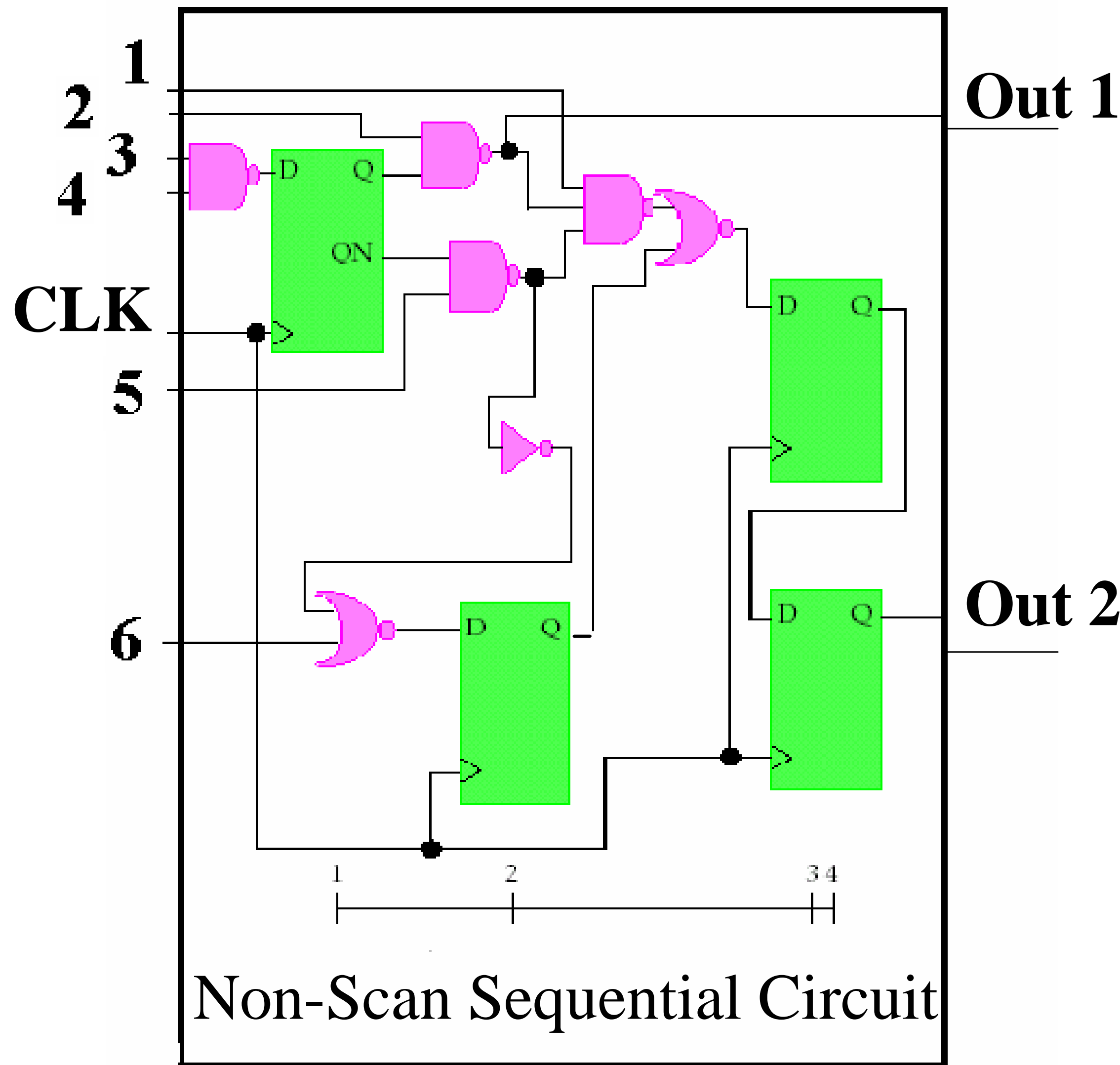
observed truth table			
A	B	C	failures
0	0	1	0
0	1	1	0
1	1	0	1
1	0	1	0

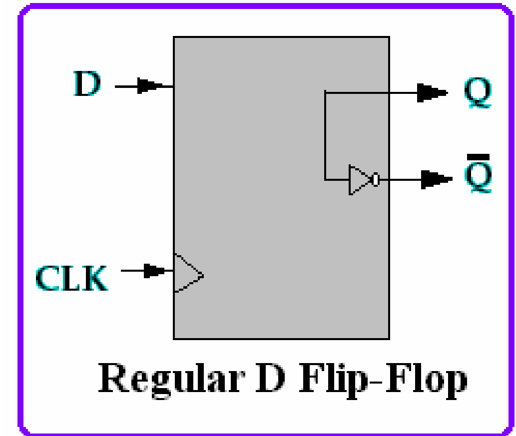
physical defects
opens shorts metal bridges process errors

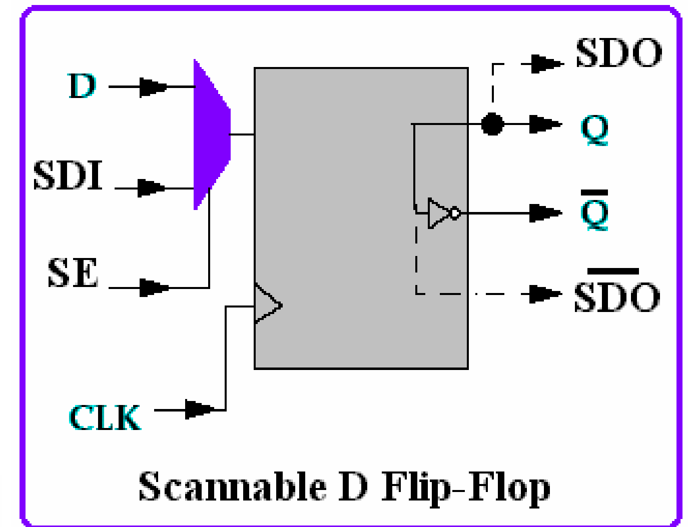
gate faults	
a@ 0	a@ 1
b@ 0	b@ 1
c@ 0	c@ 1

Scan Architecture

Inputs







Sequential depth = 4

Combinational width = 6

2^{6+4} = 1024 Test Vectors

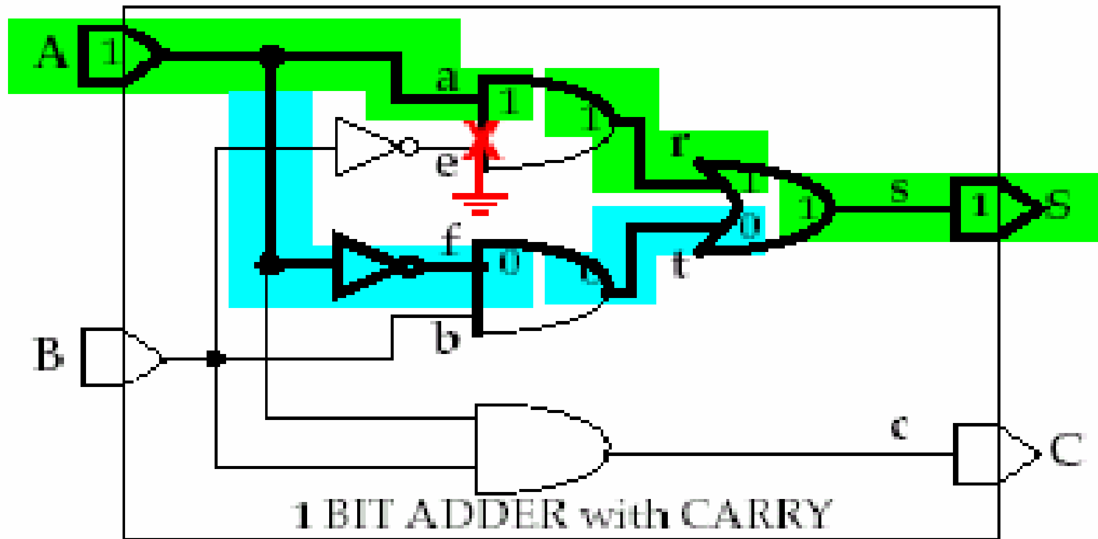
Scan Architecture

IN1
IN2
IN3
IN4
SE
Scan In
CLK
IN5
IN6
Out 1
Scan out
Out 2
SI
SI
SI
Scannable Sequential Circuit

Combinational Logic Only
Inputs
Out 1
Out 2
Scan
Inputs
Scan
Ouputs
Scan Effective Circuit

Adding Scan Structure

Test Vector Generation

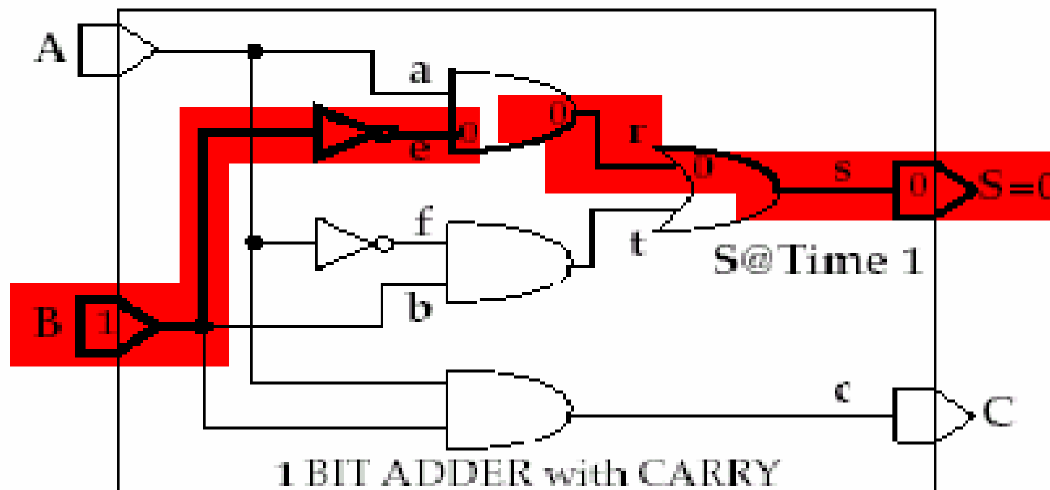


Set up the detect path (Controllability)

faultlist	
a@ 0	a@ 1
b@ 0	b@ 1
e@ 0	e@ 1
f @ 0	f @ 1
r @ 0	r @ 1
t @ 0	t @ 1
s @ 0	s @ 1
c@ 0	c@ 1
16 faults	

Test vector to cover e @ 0

In *A=1 B=0* Out *S=1*



Pass 0 to observe the fault

There are different CAD Tools to generate Test Vectors (ATPG)

RCIM: Tetramax by Synopsys

SoC test challenges

1-Deeply Embedded Cores

♦Controllability and Observability are limited.

⇒need Test Access Mechanism to transport test from source to core and from core to sink

2-Protection of Intellectual Property

∵ limited core design knowledge by chip integrator

⇒need self- contained test without core design knowledge

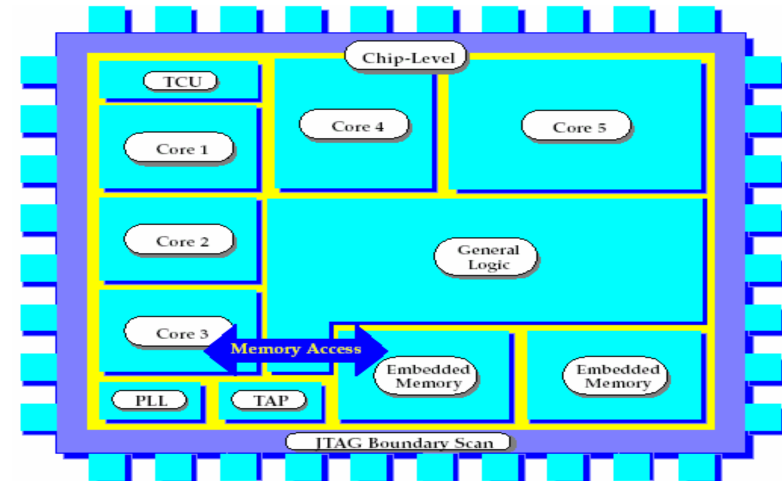
3-Limited Input/Output Bandwidth

♦ Fast data flow rates between cores inside the SoC compared to lower rates between IP cores and the external environment

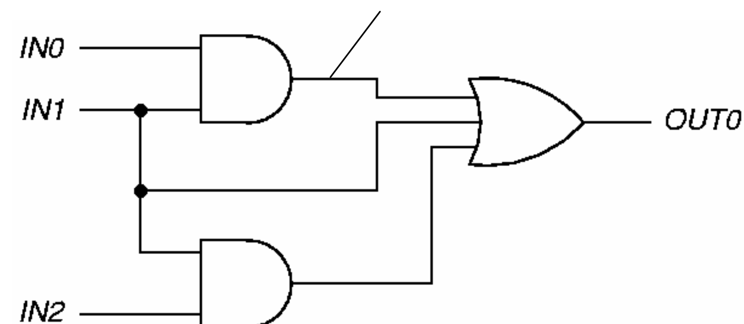
⇒ need built-in-self-test

Limited SoC Controllability and Observability

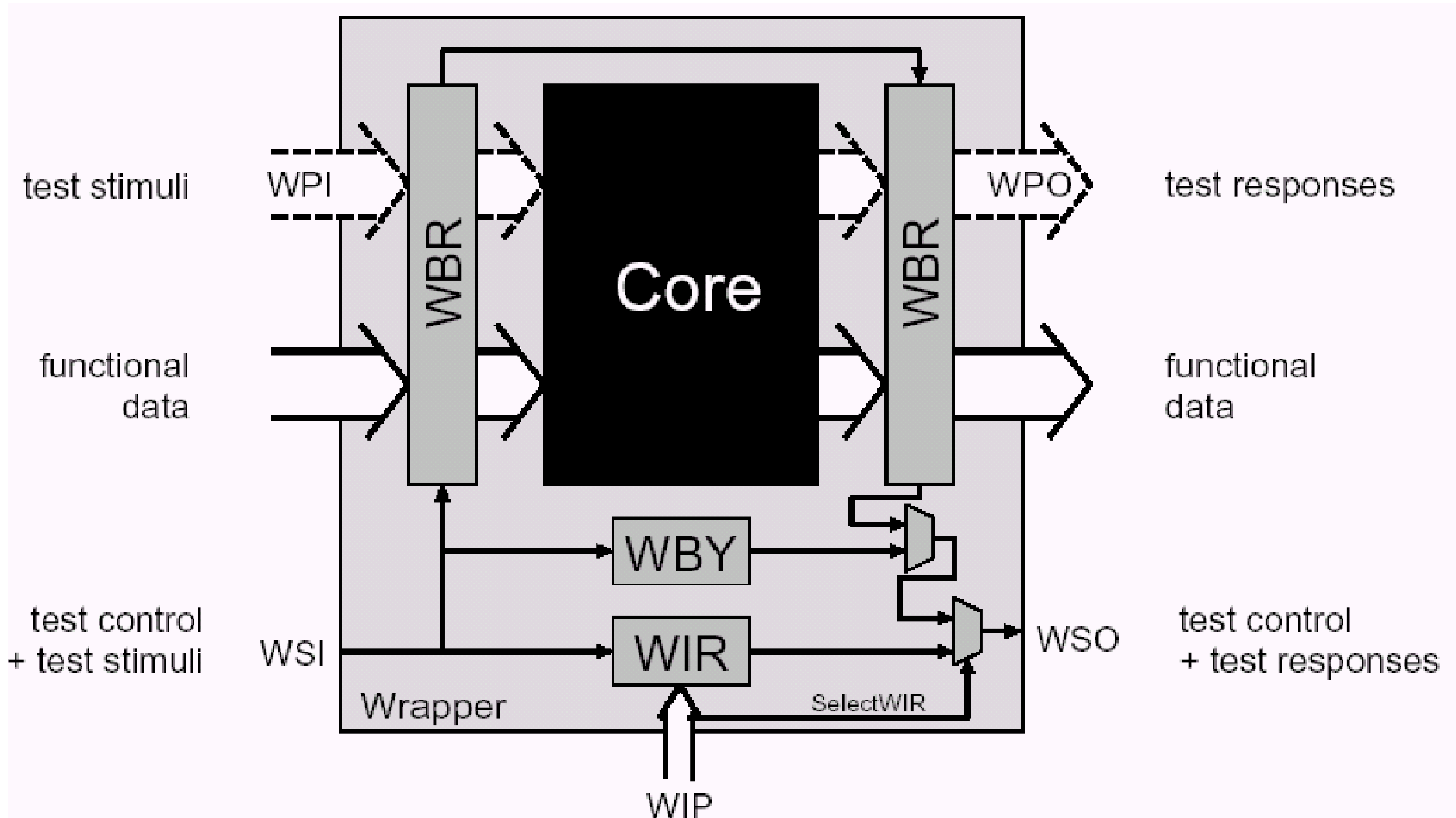
- Limited number of Pins
- Typical gates per pin =2000
- Large portion of chip would be virtually untestable even if the chip were completely combinational

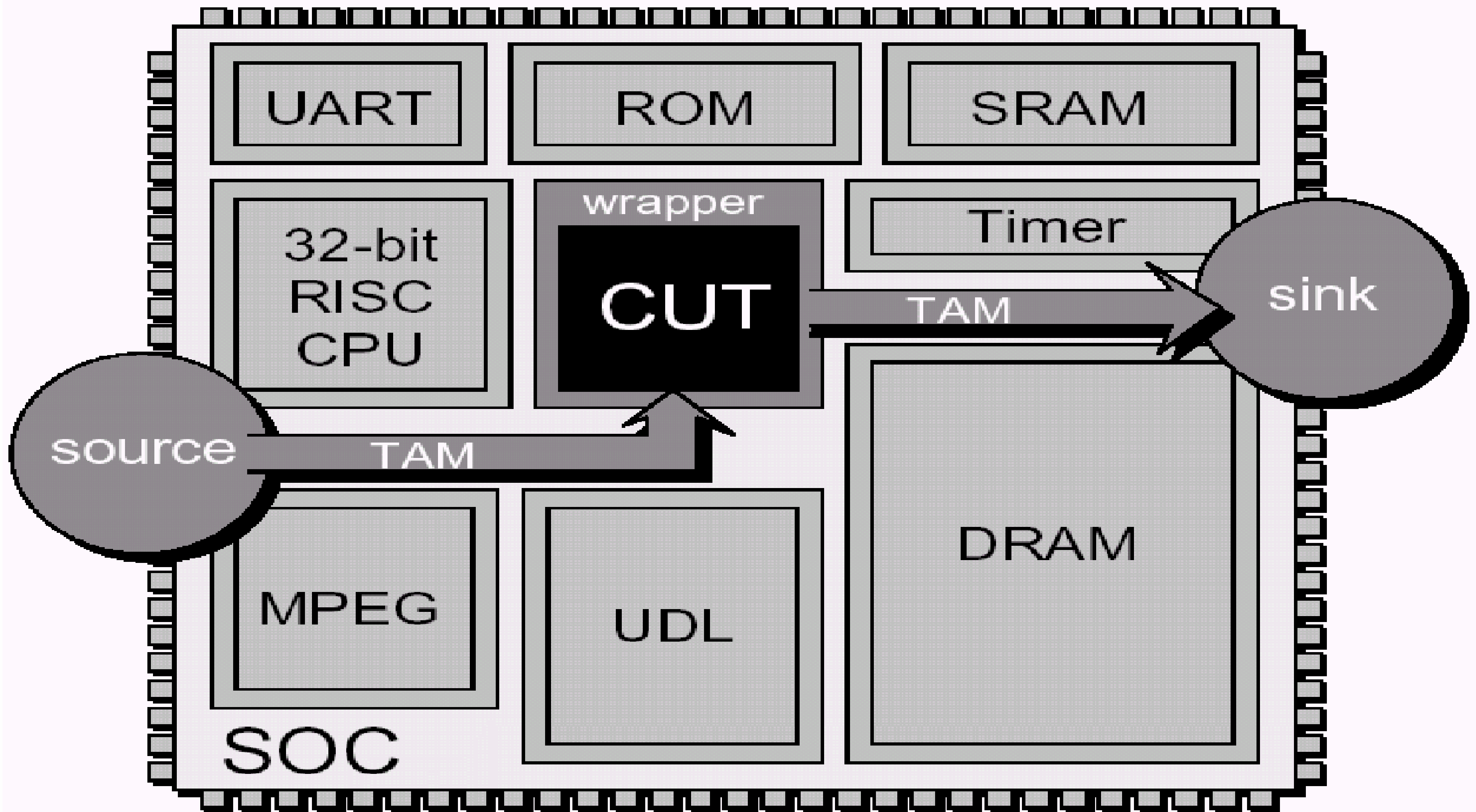


untestable



IEEE P1500 wrapper architecture



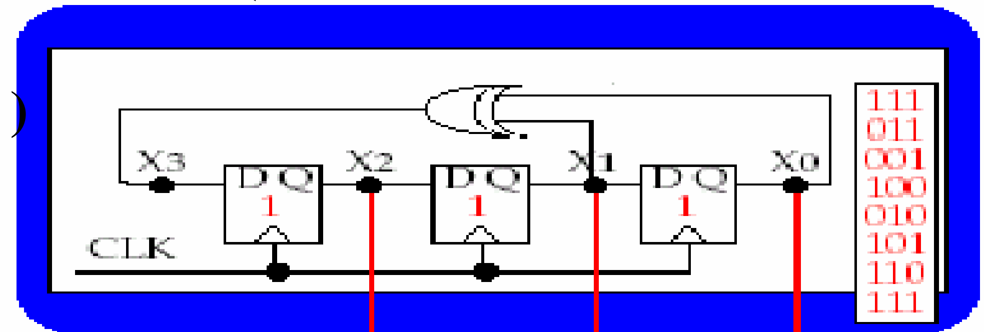


Generic test access architecture for embedded cores

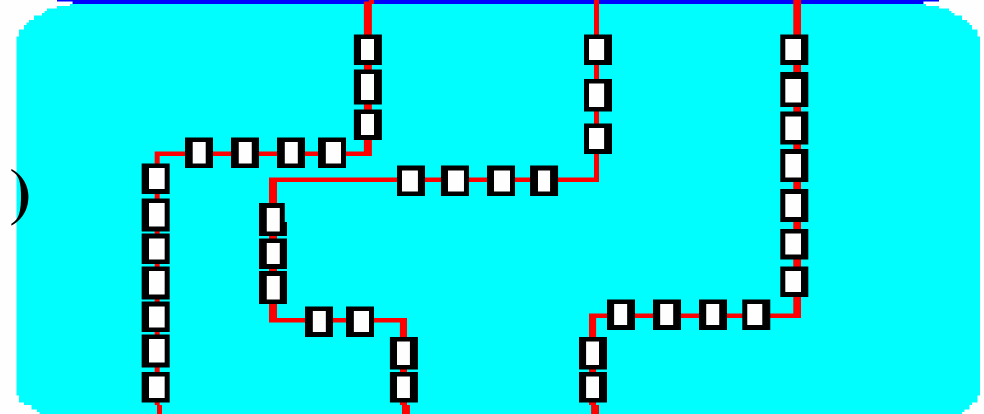
Build in Self Test (BIST)

LFSR(Linear Feedback Shift Register)

Random Test Pattern Generator

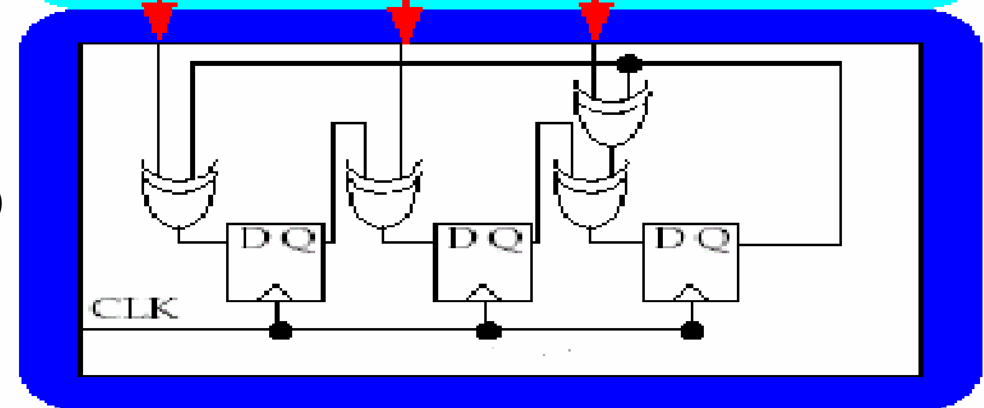


DUT (Device Under Test)



MISR (Multiple Input Shift Register)

Result Compression



Memory Build in Self Test

LFSR - PRPG

D Q D Q D Q

CLK

MBIST

Functional

5 A 0 F

MBIST Data In

Functional Data In

Algorithm Sequencer

MBIST

Functional

Functional & MBIST Data Out

Address

Memory Array

Data

Control

Data Out

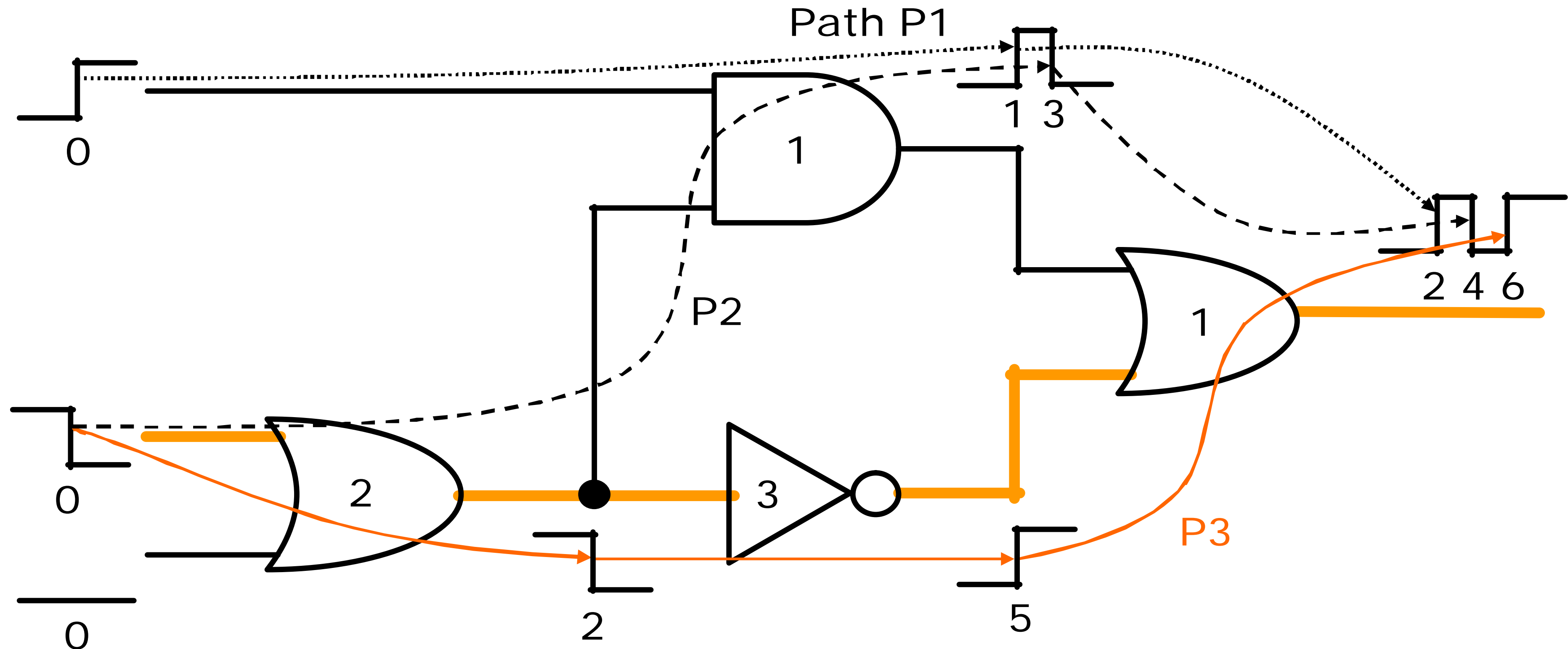
D Q D Q D Q

CLK

LFSR - MISR

LFSR-Based Memory BIST

Delay Fault



At-Speed test should perform to detect all possible delay faults.

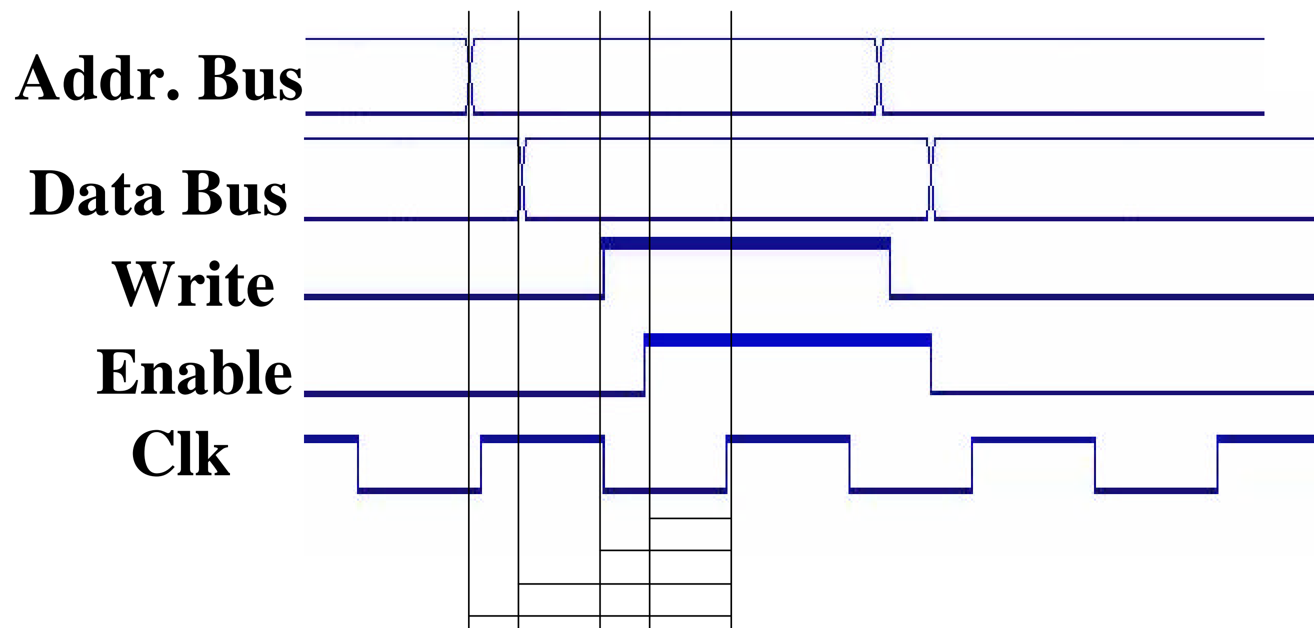
- Requires mach impedances to reduce transmission line affect
- Needs advanced and costly ATE

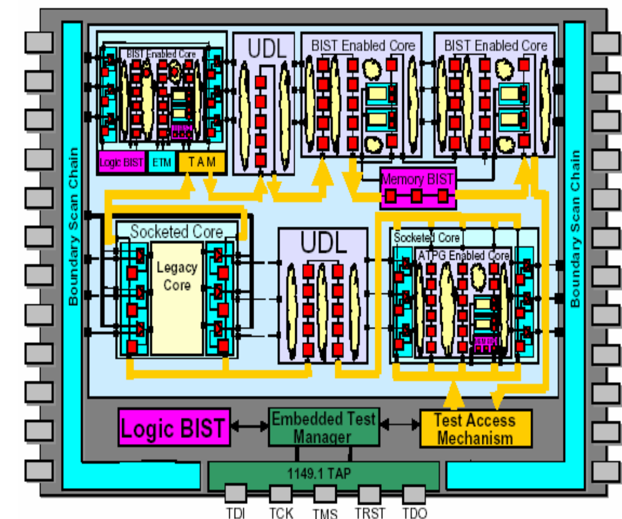
Challenges of At-Speed Testing

- **Advanced timing specification of the DUT, delay and transient faults**

  ⇒Precision timing and edge placement control for all test channels

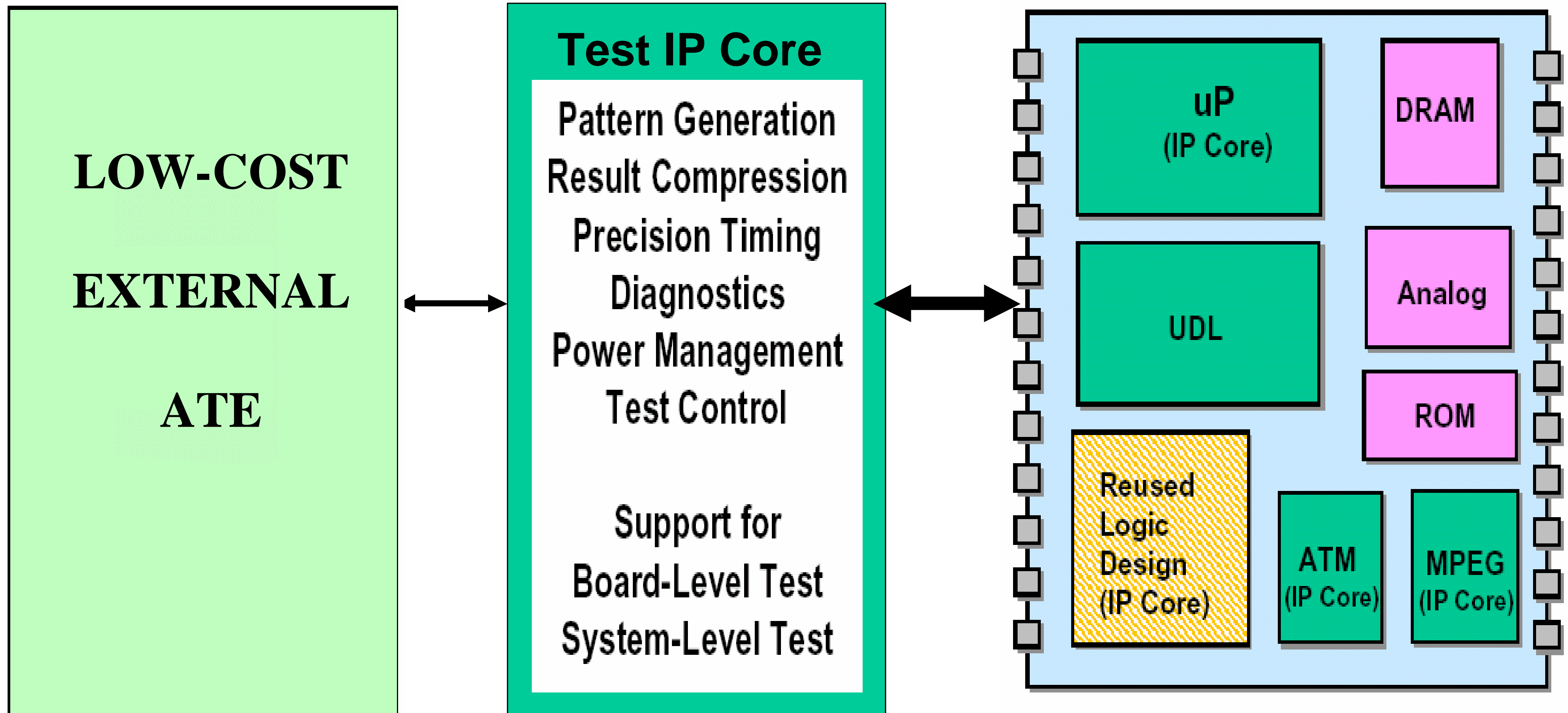
  ⇒ Require considerable memory (4M or more) behind of each test channel to carry out at_speed test





Timing constraints should be met to have a functioning circuit

Tester IP Core Architecture



External Test IP Core Embedded on MEM Socket Die

MEMS Socket Based Test Scheme

Compression Mass

Scalable Vector RAM

Die Under Test

High Bandwidth Interface

MEMS Removable Socket

Tester-on-Chip

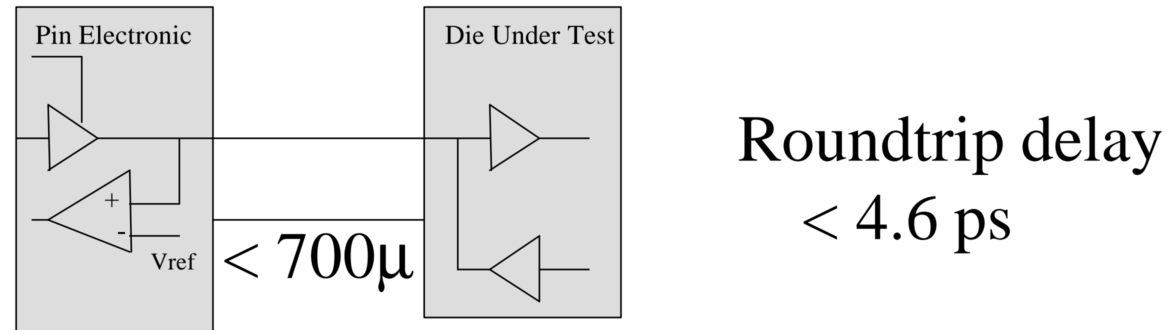
MEMS Fixed Socket

External Controller

High Bandwidth Interface

6mm

Advantages of the Proposed Test Scheme



Driver/Receiver for MEMS Based Test Head

1- Minimizes the transmission line effect problem for high speed SoC testing
2- Lowers the cost of testing significantly by reducing the required performance of the ATE
3- Reduces the packaging cost by detecting faults at the die level and removing faulty dies before the packaging process starts

ToC Design Consideration

- In the design of the Tester-on-Chip, one of the critical decisions was how to implement the on-chip timing generators for full flexibility in shaping the output waveform. The timing control circuit of the ToC allows the user to place edges near the beginning or end of the test cycle

- Separate timing generators for stimulus and response edge placement were considered for the ToC

- High speed test management circuit was designed to support at-speed test

Tester-on-Chip Building Blocks

Stimulus Waveforms Generated by ToC

Stimulus Data 0 1 1 Z 0

NRZ

RZ

RZI

RO

ROI

RTIN

RC

BIST For SoC State of the Art

1- Coherent Tester/Oscilloscope IC
- Covers delay faults and faults associated to interconnects
- Considerable area overhead

By: Dr. G. W. Roberts, McGill University

2- Oscillator-Based Test Methodology for analog circuits
- Low area overhead
- CAD tools can implement this method simply
- Can not be applied to all analog circuits

(By: B. Kaminska, Opmaxx Inc.)

3- Twisted Counter Test Method for Digital Circuits
- Generates test data for digital circuit inside the SoC
- Requires an advanced test controller

(*By: Chakrabarty, K. , Duke University*)

Research Directions

Design an embedded IP tester core optimized for analog testing in a System-on-Chip environment

- **Mathematical model of analog faults**
- **Investigating the potential of adding analog switches and switching capacitors for analog testing**
- **Developing a circuit for testing interconnects and crosstalk based on modified version of Phase Lock Loop (Delay Lock Loop)**
- **Any solution should be integratable with CAD tools**

Conclusions

- Growing gap between SoC internal and external speed makes Built-In Self-Test (BIST) a promising solution for testing

- The nature of high speed faults (e.g. transmission line affect, crosstalk,…) is analog